Amendments to the Specification

Please replace paragraph [0036] with the following:

-- Figures 6A and 6F show ~~Figure 6A shows~~ an embodiment of a system level family of equations for a PLL;--

Please replace paragraph [0037] with the following:

-- Figure 6B shows an embodiment of the variables that are called out by the family of equations of Figures 6A and 6F;--

Please replace paragraph [0042] with the following:

-- Figures 7B through 7D show ~~shows~~ circuit a topology for each of a phase detector, loop filter and feedback divider;--

Please replace paragraph [0091] with the following:

-- Figures 6a through ~~6e~~ 6f relate to an exemplary embodiment of a system level PLL description that can be "drilled down" to a transistor level of detail by employing the methodologies 500, 550 of Figures 5a and 5b. Specifically, as explained in more detail below, the system level description for the PLL may be made to include: 1) a family 600a of equations expressed in monomial or posynomial form (e.g., as seen in Figures 6a and 6f); and 2) a netlist 600d (e.g., as observed in Figure 6d), or other circuit description that describes the topology 600c of a PLL (e.g., as seen in Figure 6c). Note that the level of detail associated with the descriptions referred to just above corresponds to a system level of detail because the PLL is described (both in the equation family 600a and 600f and in the topology 600c) as a collection of basic building

blocks (i.e., phase detector, charge pump, loop filter, VCO and frequency divider).--

Please replace paragraph [0092] with the following:

--The effect(s) that the aforementioned drilling down activity will have, in terms of enabling the automatic incorporation of more detailed information into the description of the PLL, will become more apparent in the discussion that follows. Figures 6a and 6f show ~~shows~~ a representation of a family 600a and 600f of posynomial and monomial equations 621 through 629 and 631 through 638 that describe a PLL at the system level. Figure 6b shows the collection of variables and user defined values that are referred to by the family of equations 600a and 600f of Figures 6a and 6f. Figure 6c shows a system level circuit topology 600c for the PLL that may be described by a netlist (or other type of circuit description that may be used to describe a circuit topology). Figure 6d shows an embodiment of a netlist that may be used to describe the PLL topology of Figure 6c. Figure 6e shows an example of how the family of equations 600a and 600f of Figures 6a and 6f may be expanded so as to account for different operating points of the PLL.--

Please replace paragraph [0093] with the following:

--Referring to Figure 6c, the building blocks that make up the PLL 600c includes a phase detector (PFD) 601c, a charge pump (CP) 602c, a loop filter (LF) 603c, a voltage controlled oscillator (VCO) 604c and a feedback divider (DIV) 605c. Initially, an automated design tool may be tailored to configure (e.g., automatically or with the help of a designer) the system level circuit topology

600c of Figure 6c (e.g., with a netlist such as that observed in Figure 6d). Referring to either of Figures 6a, 6f, 6b, or 6c, note that (with the exception of the LF.C1, LF.C2 and LF.R terms) transistor level information is devoid from the descriptions provided therein.--

Please replace paragraph [0094] with the following:

-- As will be made apparent in subsequent sections of this application, as a result of the design tool automatically "drilling down" through multiple levels of detail, multiple threads of circuit level detail are developed. Here, each thread should extend from the high level, system representation of the PLL (e.g., as embodied in the equation set 600a and 600f in Figures 6a and 6f and the netlist 600d of Figure 6d) toward (finally) a transistor level description. Thus, in the sections following the present section, each of the PLL's building blocks 601c through 605c will be examined in greater detail. Here, an embodiment of a transistor level description (or at least a portion thereof), as implemented with additional transistor level posynomial/monomial equations and a circuit topology (from which a netlist can be readily developed) will be provided for each building block 601c through 605c. As such, the reader should be able to gain an appreciation as to how a software design tool can automatically develop a transistor level description of a PLL.--

Please replace paragraph [0095] with the following:

-- Thus, for each building block 601c through 605c, additional monomial and/or posynomial equations will be provided; wherein, these additional equations may be substituted (e.g., in accordance with the methodology 500a of

Figure 5a) into their corresponding variable within the family of equations 600a and 600f of Figures 6a and 6f (in order to expand upon the system level equation set 600a and 600f). In some cases, as examples, the result of these aforementioned substitutions will be shown so that the reader can gain an understanding into how a system level set of equations 600a and 600f for a PLL may be made to expand into greater detail as the PLL is described at (or at least closer to) a transistor level of detail. Similarly, a transistor level netlist for the loop filter 603c, a transistor level netlist for the VCO 604c and a transistor level netlist for the charge pump 602c will be substituted into the system level netlist 600d of Figure 6d (e.g., in accordance with the methodology 550 of Figure 5b) so that the reader can gain an understanding into how a system level circuit topology description may be made to expand into greater detail as the PLL is described at a transistor level of detail. As such, the description that follows is written with an eye toward the methodologies 500, 550 observed in Figures 5a and 5b.--

Please replace paragraph [0096] with the following:

-- With an understanding that a system level description may be embodied with a PLL system level netlist (e.g., as depicted in Figure 6d) that describes a PLL system topology (e.g., as depicted in Figure 6c) in terms of its constituent building blocks 601c through 605c, an examination into an embodiment of family of monomial and/or posynomial equations 600a and 600f (as depicted in Figures 6a and 6f) is presently appropriate. Referring then to Figures 6a and 6f, note that the family of equations are organized into: 1) an

equation 621 that describes the semiconductor surface area consumption of the PLL; 2) an equation 622 that describes the power consumption of the PLL; 3) a sub-family of equations 623, 624, 625, 626 that describe the static phase error of the PLL; 4) a sub family of equations 627, 628, 629, 630 that describe the output frequency of the PLL; 5) a sub family of equations 631, 632, 633, 634 that describe the stability of the PLL; 6) a pair of equations 635, 636 that describe the peak jitter of the PLL; and, 7) a pair of equations 637, 638 that describe the sensitivity of the PLL to fluctuations in the supply voltage VDD (which may be referred to as power supply rejection). A discussion of each of these follows below.--

Please replace paragraph [00106] with the following:

-- These, in turn, correspond to two different operating points that the PLL may be designed to work according to. Figure 6e illustrates the effect that multiple operating points may have on the family of monomial and posynomial equations. According to Figure 6e, as a result of a pair of operating points being specified by the designer (e.g., min PLL output frequency and max PLL output frequency), the family of monomial and posynomial equations 600a and 600f of Figures 6a and 6f may be expanded (e.g., doubled) such that the overall family of equations used for geometric problem solving 600e has a first set 600a1 that corresponds to the constraints that apply at the first operating point (e.g., the maximum allowable frequency range); and a second set 600a2 that corresponds to the constraints that apply at the first operating point (e.g., the minimum allowable frequency range).--

Please replace paragraph [00107] with the following:

--Here, note that various system level characteristics may change in light of the different operating point whereas others may not change. For example, the power consumption of the PLL should be greater at the maximum PLL output frequency than at the minimum PLL operating frequency. As such, a different numeric quantity should appear for PLL.PWR in family set 600a1 as compared to family set 600a2. Here, if the designer were to specify a maximum allowable power consumption (e.g., with a PLL.PWR_USER_SPEC input which is not indicated in Figures 6a and 6f for simplicity), the geometric problem solving process would provide a solution (if possible) that kept the power consumption within the specified range for each operating point.--

Please replace paragraph [00110] with the following:

-- Equation 632 provides an expression for the phase margin. Here, as the phase of the PLL channel is mostly determined by the loop filter and the VCO, equation 632 in expressed in terms of the loop filter components LF.R. LF.C2 and a performance characteristic of the VCO that is related to the phase delay through the VCO (VCO.TAU3). Furthermore, as the phase margin corresponds to how far above -180 degrees the phase of the PLL channel is at the cross over frequency, note that the PLL cross over frequency PLL.CROSS_OVER_FREQ also appears in equation 632. Note that the embodiment of Figures 6a and 6f allows the user to specify both the cross over frequency and phase margin (via equations 633 and 634). Specifying these parameters will impose numeric constraints on equations 631 and 632; which, in

turn, will result in a family of equations that will cause the geometric problem solving process to provide transistor level details for a PLL having the stability characteristics specified by the designer.--

Please replace paragraph [00115] with the following:

-- Figure 6b shows each of the variables that are called out by the family of equations 600a and 600f of Figures 6a and 6f. Figure 6b organizes these variables in terms of the specific building block to which they relate; or, alternatively, as a user defined variable (if the variable is to be defined by the user according to the embodiment of Figures 6a and 6f). As such, each of the variables associated with the phase detector 601b, charge pump 602b, loop filter 603b, VCO 604b and feedback divider 605b are represented in Figure 6b. Furthermore, each of the user defined variables are also listed 606b. Here, in accordance with methodology 500 of Figure 5a, the non user defined variables 601b through 605b would be recognized as having a dependency on a lower level expression (perhaps with the exception of the loop filter components LF.R, LF.C1 and LF.C2 because these may be viewed, according to some embodiments, as already being at the transistor level of detail).--

Please replace paragraph [00117] with the following:

--Figure 7a shows a monomial/posynomial equation family for the phase detector 701a, loop filter 703a, and feedback divider 705a that further describe the variables that the system level PLL description discussed in Section 6.0 depends upon; and, Figures 7b through 7d show ~~shows~~ a more detailed circuit topology embodiment 701b, 703b, 705b for each of these same building blocks,

respectively. According to an embodiment, referring to Figure 7a, a "fixed" circuit design is used for both the phase detector 701a and the feedback divider 705a. As such, the properties of these building blocks are expressed as "constants" (i.e., do not vary) rather than variables. This simply means that these building blocks are not "optimized" by the geometric problem solving process. However, their properties (as represented by constants Const_1 through Const_9) take part in the geometric solving process.--

Please replace paragraph [00118] with the following:

--That is, as constants Const_1 through Const_9 are numeric quantities that describe the corresponding characteristic to which they are labeled (e.g., Const_1 for the phase detector power, Const_2 for the phase detector area, etc.), their substitution into the PLL equation family set (e.g., as depicted in Figures 6a and 6f) will effectively add additional numeric constraints to the geometric optimization problem. Better said, the geometric problem solving process will attempt to optimize the charge pump components, loop filter components and VCO components in light of the numeric constraints (Const_1 through Const_9) that are imposed by use of a pre-configured, "fixed" phase detector and frequency divider design. This approach may be used if it is believed that the charge pump and frequency divider (perhaps because they make use of digital circuitry) do not add much to the overall optimization issue.--

Please replace paragraph [00121] with the following:

-- Referring to the circuit topologies 701b, 703b, and 705b of Figures 7b, 7c, and 7d, respectively ~~Figure 5b~~, those of ordinary skill may readily develop a

transistor level netlist for each. Here, according to the embodiment discussed above wherein the phase detector and feedback divider are fixed, a netlist (e.g., in HSPICE format) for each of these building blocks is included with the design tool software (e.g., as part of a database) so that they may be substituted into the system level netlist of the PLL (e.g., as depicted in Figure 6d) in accordance with methodology 550 of Figure 5b. Likewise, a netlist that describes the topology of the loop filter 703b may also be included with the design tool software. More detail regarding the automatic expansion of the PLL netlist are described below in Section 7.0.--

Please replace paragraph [00122] with the following:

--Figure 8a shows an embodiment of a family of monomial/posynomial equations 820 through 826 that describe the charge pump variables that the PLL system level description embodiment of Figures 6a and 6f is dependent upon (as summarized in table 602b of Figure 6b). Here, note that equations 820 and 822 through 826 are posynomial; and, equation 821 is monomial. Figure 8b shows additional equations 802b (in posynomial and/or monomial form) that can be added to the family of equations for geometric problem solving. Here, the equations of Figure 8b describe the "DC biasing" conditions of the charge pump circuit. An embodiment of a charge pump circuit 802c to which both sets of equations 802a, 802b relate is shown in Figure 8c.--

Please replace paragraph [00131] with the following:

--Figure 9a shows an embodiment of a family of monomial/posynomial equations 920 through 925 that describe the VCO variables that the PLL system

level description embodiment of Figures 6a and 6f is dependent upon (as summarized in table 602b of Figure 6b). Here, note that equations 920, 921 and 923, 924 are posynomial while equation 922 and 925 are monomial (noting that the expression $\mu n + \mu p$ is a constant as described in more detail below). Figure 9b shows additional equations 905b (in posynomial and/or monomial form) that can be added to the family of equations for geometric problem solving. Here, the equations of Figure 9b describe the "DC biasing" conditions of the VCO. An embodiment of a VCO circuit 802c to which both sets of equations 902a, 902b relate is shown in Figure 9c.--

Please replace paragraph [00139] with the following:

-- Figure 10 shows an embodiment of a methodology 100 by which an automated design tool designed according to the principles expressed above may be configured to operate according to. Initially a system level description of a PLL is created 1001. Recall that an example of a system level description was discussed with respect to Figures 6a through ~~6e~~ 6f. Here, the construction of a system level description results in system level topology information 1006 (e.g., the netlist of Figure 6d) and system level monomial and/or posynomial equations 1007 (e.g., a example of which were shown in Figures 6a and 6f).--

Please replace paragraph [00143] with the following:

--Figure 12 ~~provide~~ provides a specific example as to how the PLL's family of equations become more detailed with each substitution. Figure 12 shows the original system level equation for PLL power consumption (as expressed in Figures 6a and 6f). Equation 1201 of Figure 12, shows this same equation after

the CP.PWR term is substituted with equation 820 of Figure 8a and the VCO.PWR term is substituted with equation 920 of Figure 9. Here, note that equation 1201 effectively describes the PLL's power consumption in greater detail by expanding on each of the CP.PWR and VCO.PWR terms with transistor level expressions. Likewise, for each of the non user defined variables of Figure 6b, a similar substitution could be made which would result in the entire PLL being described at a greater level of detail.--

Please replace paragraph [00144] with the following:

-- Figure 13 shows an example as to how the system level netlist can be made to be more detailed as lower level circuit toplogy information is substituted into the system level netlist. Figure 13 shows the simple case of the changes made to the system level netlist of Figure 6d if the circuit topology information of the loop filter of Figure ~~7b~~ 7c is substituted in. Here, note that nodes 6 and 7 of the system level netlist of Figure 6d are merged because the loop filter topology of Figure ~~7b~~ 7c indicates that the input and output of the loop filter are the same node. As such, whereas the CP.OUT and VCO.IN nodes were on different nets in the system level description of Figure 6D, they now share the same node in the more detailed netlist of Figure 13. Furthermore, whereas the system level netlist of Figure 6d is devoid of specific resistor and capacitor values (which are considered a low level of detail), note that this information appears when the loop filter specifics are accounted for. Specifically, nodes 2, 6, and 7 ~~contains~~ contain specific resistance and capacitance details (noting that node 7 was reconfigured so as to correspond to the node between R and C1). Similar to the

discussion above with respect to Figure 12, each insertion of more detailed topological information (e.g., the design for the charge pump or VCO as provided in Figures 8c and 9c) will add more nodes and more complexity to the netlist (which corresponds to the netlist being described at a greater level of detail).--